3. (Twice Amended) The circuit according to claim 1 wherein the write charge control circuit transfers charge between at least one of the first and second data IO lines and a bit line.

4. The circuit according to claim 1 wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

5. The circuit according to claim 4 wherein the first and second write controlled gates are both controlled by a write column select line signal.

6. (Twice Amended) The circuit according to claim 4 wherein the first write controlled gate is coupled directly between the bit line and the first data IO line and the second write controlled gate is coupled directly between the complementary bit line and the second data IO line.

7. (Twice Amended) The circuit according to claim 1 wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to the second data IO line and a second read controlled gate controlling charge from a complementary bit line to the first data IO line.

8. The circuit according to claim 7 wherein the first and second read controlled gates are both controlled by a read column select line signal.

9. (Twice Amended) The circuit according to claim 7 wherein the first read controlled gate is coupled directly between the bit line and the second data IO line and the second read controlled gate is coupled directly between the complementary bit line and the first data IO line.

10. (Twice Amended) The circuit according to claim 1 including a data output sense amplifier coupled between a data output buffer and the first and second data IO lines.

11. The circuit according to claim 10 including load transistors shared between the read charge control circuit and the data output sense amplifier.

12. (Twice Amended) The circuit according to claim 1 wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to the second data IO line, and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to the first data IO line, and a third terminal; and

a third transistor having a first terminal coupled to a column select line, a second terminal coupled to the third terminal of the first and second transistor, and a third terminal coupled to a first reference voltage.

3) cont'd.

13. (Twice Amended) The circuit according to claim 12 wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to a write column select line, a second terminal coupled to the complementary bit line, and a third terminal coupled to the second data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the first data IO line, and a third terminal coupled to the bit line.

14. (Twice Amended) The circuit according to claim 13, further comprising:

a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the first data IO line, and a third terminal coupled to a third reference voltage; and

a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the second data IO line, and a third terminal coupled to the third reference voltage.

15. A circuit, comprising:

a read charge control circuit activated by a read column select line;

a write charge control circuit activated by a write column select line, wherein the read charge control circuit and the write charge control circuit are both coupled to common data IO lines;

a data output sense amplifier; and

B1 cont'd. load transistors shared by both the read charge control circuit and the data output sense amplifier.

34. The circuit of claim 15, wherein the write charge control circuit is activated independently of the read column select line used for activating the read charge control circuit.

35. The circuit of claim 15, wherein the read charge control circuit is a sense amplifier.

36. The circuit of claim 15, wherein the write charge control circuit transfers charge between the common data IO lines and bit lines.

B2 37. The circuit of claim 15, wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

38. The circuit of claim 37, wherein the first and second write controlled gates are both controlled by a write column select line signal.

39. The circuit of claim 37, wherein the first write controlled gate is coupled directly between the bit line and data IO line and the second write controlled gate is coupled directly between the complementary bit line and a complementary data IO line.

40. The circuit of claim 15, wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to a complementary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line.

41. The circuit of claim 40, wherein the first and second read controlled gates are both controlled by the read column select line.

42. The circuit of claim 40, wherein the first read controlled gated is coupled directly between the bit line and the complementary data IO line and the second read controlled gate is coupled directly between the complementary bit line and the data IO line.

43. The circuit of claim 15, wherein the data output sense amplifier is coupled between a data output buffer and the common data IO lines.

44. The circuit of claim 15, wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to a complementary data IO line and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal; and

a third transistor having a first terminal coupled to the read column select line, a second terminal coupled to the third terminal of the first and second transistors and a third terminal coupled to a first reference voltage.

45. The circuit of claim 44, wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to the write column select line, a second terminal coupled to the complementary bit line and a third terminal coupled to the complementary data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line.

46. The circuit according to claim 45 including

a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage; and

a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the complementary data IO line and a third terminal coupled to the third reference voltage.

47. (New) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address, the read charge control circuit coupled to a first and a second data IO line, wherein the second data IO line is complementary to the first data IO line; and

a write charge control circuit activated by a write signal and the same or a different address, the write charge control circuit coupled to the first and the second data IO line, wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

48. (New) The circuit of claim 47, wherein the first and second write controlled gates are both controlled by a write column select line signal.

49. (New) The circuit of claim 47, wherein the first write controlled gate is coupled directly between the bit line and the first data IO line and the second write controlled gate is coupled directly between the complementary bit line and the second data IO line.

50. (New) A circuit, comprising:

a read charge control circuit that is activated only during read operations by a read signal and an address,

wherein the read charge control circuit is coupled to a first and a second data IO line,

wherein the second data IO line is complementary to the first data IO line, and

wherein the read charge control circuit includes a first read control gate that controls charge from a bit line to the second data IO line and a second read control gate that controls charge from a complementary bit line to the first data IO line; and

a write charge control circuit activated by a write signal and the same or a different address, wherein the write charge control circuit is coupled to the first and the second data IO line.

51. (New) The circuit of claim 50, wherein the first and second read control gates are both controlled by a read column select line signal.

52. (New) The circuit of claim 50, wherein the first read control gate is coupled directly between the bit line and the second data IO line and the second read control gate is coupled directly between the complementary bit line and the first data IO line.

53. (New) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address and coupled to a first and a second data IO line, wherein the second data IO line is complementary to the first data IO line;

a write charge control circuit activated by a write signal and the same or a different address, the write charge control circuit coupled to the first and the second data IO line;

a data output sense amplifier coupled between a data output buffer and the first and second data IO lines; and

load transistors shared between the read charge control circuit and the data output sense amplifier.

54. (New) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address and coupled to a first and a second data IO line, wherein the second data IO line is complementary to the first data IO line, and

a write charge control circuit activated by a write signal and the same or a different address, the write charge control circuit coupled to the first and the second data IO line;

wherein the read charge control circuit comprises

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to the second data IO line, and a third terminal;

a second transistor having a fourth terminal coupled to a complementary bit line, a fifth terminal coupled to the first data IO line, and a sixth terminal; and

a third transistor having a seventh terminal coupled to a column select line, an eighth terminal coupled to the third terminal and the sixth terminal, and a ninth terminal coupled to a first reference voltage.

55. (New) The circuit of claim 54, wherein the write charge control circuit comprises:

a fourth transistor with a tenth terminal coupled to a write column select line, an eleventh terminal coupled to the complementary bit line, and a twelfth terminal coupled to the second data IO line; and

a fifth transistor with a thirteenth terminal coupled to the write column select line, a fourteenth terminal coupled to the first data IO line, and a fifteenth terminal coupled to the bit line.

56. (New) The circuit of claim 54, further comprising:

a first load transistor having a sixteenth terminal coupled to a second reference voltage, a seventeenth terminal coupled to the first data IO line, and an eighteenth terminal coupled to a third reference voltage; and

a second load transistor having a nineteenth terminal coupled to the second reference voltage, a twentieth terminal coupled to the second data IO line, and a twenty-first terminal coupled to the third reference voltage.